Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.615”**



**.512”**

**Top Material: Al**

**Backside Material: TiNiAu**

**Bond Pad Size: .004” X .004”**

**Backside Potential: DRAIN**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .512” X .615” DATE: 7/21/21**

**MFG: IXYS THICKNESS .016” P/N: IXFD55N50**

**DG 10.1.2**

#### Rev B, 7/19/02